AMENDMENTS TO THE CLAIMS

The following is a complete, marked up listing of revised claims with a status identifier in parentheses, underlined text indicating insertions, and strikethrough and/or double-bracketed text indicating deletions.

LISTING OF CLAIMS

1-12 (CANCELED)

13. (ORIGINAL) A capacitor of a semiconductor device comprising:

an interlayer dielectric pattern disposed on a semiconductor substrate, the interlayer dielectric pattern having an opening, the opening exposing a surface region of the semiconductor substrate;

a silicide pattern formed on the surface region of the semiconductor substrate exposed through the opening;

a lower electrode covering an inner wall of the opening and the silicide pattern;

a dielectric layer covering an inner wall and a top surface of the lower electrode; and

an upper electrode disposed on the dielectric layer.

14. (ORIGINAL) A capacitor of a semiconductor device according to claim 13, wherein the silicide pattern comprises at least one material selected from a group consisting of titanium silicide and cobalt silicide.

15. (ORIGINAL) A capacitor of a semiconductor device according to claim 13, wherein the lower electrode comprises at least one conductive material selected from a group consisting of titanium nitride, tungsten and ruthenium.

16. (ORIGINAL) A capacitor of a semiconductor device according to claim 13, further comprising a heavily doped region formed in the semiconductor substrate under the opening.

17. (ORIGINAL) A capacitor of a semiconductor device according to claim 13, wherein the dielectric layer comprises at least one dielectric material selected from the group consisting of tantalum oxide, aluminum oxide, titanium oxide, silicon oxide, silicon nitride, hafnium oxide, BST (Barium Strontium Titanate), and PZT (Lead Zirconium Titanate).

18. (ORIGINAL) A method of fabricating a capacitor on a semiconductor device comprising:

providing a semiconductor substrate;

forming a interlayer dielectric layer on the semiconductor substrate;

forming a interlayer dielectric pattern, the interlayer dielectric pattern comprising an opening, the opening comprising an inner wall and exposing a predetermined surface region of the semiconductor substrate;

forming a metal layer on the interlayer dielectric pattern;

forming a lower electrode layer on the metal layer;

forming a lower electrode on the inner wall of the opening and the predetermined surface region of the semiconductor substrate;

forming a dielectric layer on the lower electrode; and

forming an upper electrode layer on the dielectric layer.

19. (PREVIOUSLY PRESENTED) A capacitor of a semiconductor device comprising:

an interlayer dielectric pattern disposed on a semiconductor substrate, the interlayer dielectric pattern having an opening that exposes a surface region of the semiconductor substrate, wherein an upper surface of the interlayer dielectric pattern defines a first plane and the opening has an inner surface and a depth D_o;

a silicide pattern formed on the exposed surface region of the semiconductor substrate;

a lower electrode covering the inner surface of the opening and the silicide pattern with an upper portion of the lower electrode projecting above the first plane by a height H_e, wherein a ratio of D_o:H_e is no greater than 10:1;

a dielectric layer having a first portion covering exposed surfaces of the lower electrode and a second portion extending across the upper surface of the dielectric pattern; and

an upper electrode covering the first portion of the dielectric layer and a region of the second portion of the dielectric layer adjacent the opening.

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